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Reg. No. : .....

Name : .....

Fifth Semester B.Tech. Degree Examination, November 2013
(2008 Scheme)
08.503 : COMPUTER ORGANISATION AND ARCHITECTURE (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Explain the addressing modes in MIPS.
2. What is biased notation ?
3. Compare RISC and CISC processors.
4. Consider 3 processors with same instruction set with clock rates and CPI given below.

	Clock Rate (Ghz)	CPI
P1	2	1.5
P2	1.5	1.0
P3	3	2.5

   a) Which processor has highest performance ?

   b) If the processors each execute a program in 10 s, find the number of cycles and number of instructions.

5. Draw the datapath for branch instruction in MIPS implementation.
6. Explain structural hazards with an example.
7. Give the methods for improving cache performance.
8. Compare write through and write back scheme.
9. Explain Memory system hierarchy.
10. What is Memory interleaving ?

(10×4=40 Marks)

P.T.O.

PART – B

Answer **any two** questions from **each** Module.

Module – I

11. Write the MIPS assembly code for the following C code.

```
void strcpy (char x [ ], char y [ ])
{  int i ;
   i = 0 ;
   while (x[i] = y[i] 1 = '\0')
     i + = 1;
}
```

x and y are array of bytes and Base addresses for arrays x and y are found in $ a_0 and $ a_1. i is in $ s_0.

12. a) Explain the different types of instructions in MIPS.
    b) Show the IEEE 754 binary representation of the number $(-0.75)_{10}$ in single and double precision.

13. With an example, explain the algorithm for binary division.

Module – II

14. Explain the datapath for basic memory reference instructions in MIPS in single clock cycle implementation.
15. With the help of diagram and necessary control signals, explain multicycle implementation scheme.
16. Explain the various pipeline hazards and the methods used to eliminate them.

Module – III

17. Explain the architecture of 8086.
18. a) Explain DMA Data transfer.
    b) Discuss the address translation in virtual memory.
19. a) How many bits are required for a direct mapped cache with 16 KB of data and 4-word blocks, assuming a 32 bit address ?
    b) Explain the different mapping techniques in cache memory. **(6×10=60 Marks)**